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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
MYERS, PAUL R	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 09/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/839,768	LIAW ET AL.	
	Examiner	Art Unit	
	Paul R. Myers	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *46-67* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *46-67* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 46-67 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 46, 47, 49-50, 53-54, 56 and 58 rejected under 35 U.S.C. 102(b) as being anticipated by Protigal et al PN 5,307,309.

In regards to claim 46: Protigal et al teaches (in the prior art) A memory module (101), comprising: a first circuit board (103) including a first conductive trace (lead) disposed on a surface of the first circuit board; a first connector (107 for Vcc) including at least one contact connected to the first conductive trace, wherein the first connector is for removably connecting the first circuit board to a second circuit board (inherent the motherboard onto which the SIMM is plugged); and a first capacitor (21) including: one capacitor electrode connected to the first connector at a junction where the contact connects to the first conductive trace (at Vcc); and another capacitor electrode coupled to a node that is at a supply potential (Ground).

In regards to claims 47, 49: Protigal et al's connectors are edge connectors.

In regards to claim 50: Protigal et al also teaches a pin (Figure 11).

In regards to claim 53: Protigal et al teaches the supply potential being ground potential.

In regards to claim 54: Protigal et al teaches a ground plain parallel to and beneath the surface or the board (Column 2 lines 58-66).

In regards to claim 56: Protigal et al teaches pad and signal lines being of different sizes thus they would have different impedance values.

In regards to claim 58: Protigal et al teaches memory devices.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 48 is rejected under 35 U.S.C. 103(a) as being unpatentable over Protigal et al PN 5,307,309 in view of Dell et al PN 5,513,135.

In regards to claim 48: Protigal et al teaches the contacts are disposed on the surface but is silent as to whether or not the contacts are on both surfaces as is standard. Dell et al teaches edge contacts on the front and back surfaces. It would have been obvious to a person of ordinary skill in the art at the time of the invention to have allowed for a greater number of contacts thus greater addressing or alternatively more surface area for contacting thus preventing an open circuit.

4. Claim 51 is rejected under 35 U.S.C. 103(a) as being unpatentable over Protigal et al PN 5,307,309 in view of Shepherd PN 4,781,624.

In regards to claim 51: Protigal et al teaches the capacitor being on the daughter board as opposed to the motherboard. Shepherd teaches capacitors being on the board into which a device is to be plugged as opposed to the board of the device. It would have been obvious to a person of ordinary skill in the art to place the decoupling capacitor on the motherboard because this would have prevented the capacitors from taking up space on the daughter board.

5. Claims 52 and 55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Protigal et al PN 5,307,309 in view of Dougherty et al PN 4,439,813.

In regards to claim 52: Protigal et al teaches a discrete capacitor but is silent upon the form the capacitor takes. Dougherty et al teaches a decoupling capacitor with the plates being conductive pads on the board. It would have been obvious to use Dougherty et al's capacitors because this would have allowed for a reduced capacitor footprint.

In regards to claim 55: Protigal et al teaches the circuit board with a ground plane as described above. Protigal is silent upon the existence of a dielectric disposed between the surface and ground plane. Dougherty et al expressly teaches a dielectric between the surface and the ground plane.

6. Claims 57 is rejected under 35 U.S.C. 103(a) as being unpatentable over Protigal et al PN 5,307,309 in view of Kledzik PN 5,266,912.

In regards to claim 57: Protigal et al's capacitor is for decoupling as opposed to impedance matching. Kledzik teaches it is desirable to perform impedance matching on SIMM memory modules. Capacitors are commonly used in impedance matching. It would have been

obvious to use a capacitor for impedance matching in the memory module of Protigal et al because this would have prevented signal reflection (the reason for impedance matching).

7. Claims 59 is rejected under 35 U.S.C. 103(a) as being unpatentable over Protigal et al PN 5,307,309 in view of Burger et al PN 4,788,766.

In regards to claim 59: Protigal is silent as to the type of signal traces. Burger teaches multiple types of signal traces such as stripline and microstrip. It would have been obvious to use microstrip as the trace because this is a standard type of signal trace.

8. Claims 60-61 are rejected under 35 U.S.C. 103(a) as being unpatentable over Protigal et al PN 5,307,309 in view of Kledzik PN 5,266,912 as applied to claim 57 and further in view of Geiszler PN 3,359,510.

In regards to claims 60-61: Kledzik teaches handling impedance matching. Kledzik does not teach varying the width of the conductor for impedance matching. Geiszler teaches varying the width of a conductor for impedance matching. It would have been obvious to a person of ordinary skill in the art to use width varying for impedance matching because this would have allowed for handling microwave frequency.

9. Claims 62-67 is rejected under 35 U.S.C. 103(a) as being unpatentable over Protigal et al PN 5,307,309 in view of Kledzik PN 5,266,912 as applied to claim 57 and further in view of Shepherd PN 4,781,624.

In regards to claim 62: Protigal in view of Kledzik teaches a capacitor attached to the inserted circuit board for impedance matching as described above. Shepherd teaches a capacitor attached to the base circuit board for noise filtering as described above. It would have been obvious to include a capacitor on both circuit boards because this would have allowed for impedance matching and noise filtering.

In regards to claim 63: Protigal et al teaches the capacitor being on the daughter board. Shepherd teaches capacitors being on the board into which a device is to be plugged (Motherboard).

In regards to claim 64: Protigal et al teaches the memory module being a SIMM which inherently is orthogonal to the surface of the motherboard.

In regards to claim 65: Shepherd teaches the capacitor is for noise reduction. Shepherd does not teach the capacitor affects impedance. Kledzik teaches (figure 20 and Column 3 lines 34 to Column 4 line 12) impedance matching and the capacitance values chosen should be for optimum impedance matching. it would have been obvious to chose a capacitance that provides impedance matching as the second capacitor because this would have provided for minimum impedance differential thus minimized signal reflection and thus minimized noise which by the way is the purpose of Shepherd.

In regards to claim 66: Protigal and Shepherd both teach conductive pads. Protigal teaches edge connectors.

In regards to claim 67: Shepherd teaches right angle turns at the ends of conductive traces.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

PN 5,734,208 to Jones teaches every claimed feature of the independent claim.

PN 4,879,631 to Johnson teaches every claimed feature of the independent claim.

PN 5,432,916 to Hahn et al teaches the claimed subject matter except the unit is not a memory module.

PN 4,473,755 to Imai et al teaches the claimed subject matter except the unit is not a memory module.

PN 5,189,638 to Kimura teaches the claimed subject matter except the second capacitor electrode is not at a supply potential.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul R. Myers whose telephone number is 571 272 3639. The examiner can normally be reached on Mon-Thur 6:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul R. Myers

PRM
July 7, 2005

PAUL R. MYERS
PRIMARY EXAMINER